#7

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Substitute for Form PTO-1449

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Complete if known	
Application Number	09/691,406
Filing Date	October 17, 2000
First Named Inventor	Christopher Hoover
Group Art Unit	Not yet assigned
Examiner Name	Not yet assigned
Attorney Docket Number	21891.02500

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (if known)	Name of Patentee or Applicant Of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
[signature]	A1	5,963,447		Kohn et al.	10/05/1999	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Foreign Patent Document Number[4]	Foreign Patent Document Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[6]
[signature]	C1 ✓	Rogers, P. et al. (1997) "A Simulation Testbed for Comparing the Performance of Alternative Control Architectures," *Proceedings of the 1997 Winter Simulatin Conference*, pp. 880-887	
[signature]	C2 ✓	Oreizy, P. et al. (1999) "An Architecture-Based Approach to Self-Adaptive Software," *IEEE Intelligent Systems*, **14**(3):54-62	
[signature]	C3 ✓	Clarke, P. (1999) "Cadence Virtual Component Codesign Tools Set for January Release," *Electronic Engineering Times*, **1087**:80	
[signature]	C4 ✓	Santarini, M. (2000) "Cadence Rolls System-Level Design to Fore," *Electronic Engineering Times*, **1095**:pp. 1, 22, 24 and 130	

Examiner Signature	[signature]	Date Considered	03/31/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation is not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

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PTO/SB/08b(05-03)
Approved for use through 04/30/2003. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if Known	
Application Number	09/691,406
Filing Date	October 17, 2000
First Named Inventor	Christopher Hoover
Group Art Unit	2123
Examiner Name	Not assigned
Attorney Docket Number	21891.02500

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	AA	CASSAGNOL, BOB; et al., "Codesigning a Complex System on a Chip with Behavioral Modesl," November 1998, http://2www.isdmag.com/Editorial/1998/coverstory9811.html, 3/18/00.	
	AB	Cadence website, Cadence Press Release, "Addressing the Systems-in-Silicon Verification Challenge," http://www.cadence.com/press_box/na/pr/1995/inca.html, 3/18/00	
	AC	Cadence website, "System-Level design," http://www.cadence.com/technology/hwsw/vcc/html, 3/18/00	
	AD	Cadence website, "System-Level design," http://www.cadence.com/technology/hwsw/, 3/18/00	
	AE	Cadence website, "Digital Block Implementation," http://www.cadence.com/technology/digital/, 3/18/00	
	AF	Cadence website, "Functional Design and Verification," http://www.cadence.com/technology/funct/, 3/18/00	
	AG	Cadence website, "Custom Block Implementation," http://www.cadence.com/technology/custom/, 3/18/00	
	AH	Cadence webstie, "Physical Verification, Extraction and Analysis," http://www.cadence.com/technology/phys/, 3/18/00	
	AI	Cadence website, "Chip Planning and Assembly," http://www.cadence.com/technology/chip/, 3/18/00	
	AJ	Cadence webstie, "PCB Design and IC Packaging," http://www.cadence.com/technology/pcb, 3/18/00	
	AK	WILSON, LES and CRITTEN, JEFF, "White Paper: DSP SOC Design Methodology for Digital Camera," 2000, Cadence Design Systems, Inc.	

Examiner Signature		Date Considered	03/31/2006

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